WHAT IS CLAIMED IS:

1. A circuit comprising:

a plurality of driver slices, a portion of the plurality of the driver slices being used to provide a target impedance;

a digital matching logic to select the portion of the plurality of the driver slices; and

an analog matching circuit to produce a bias voltage to match pull-up and pull-down.

2. The circuit of claim 1 wherein the digital matching logic selects the portion of the plurality of the driver slices based on one or more items selected from a group comprising a target impedance and a reference resistor.

3. The circuit of claim 2 wherein the target impedance is determined through a dial-in code.

4. The circuit of claim 2 wherein the target impedance is selected based on one or more items selected from a group comprising a calibrated source and a look-up table.

5. The circuit of claim 1 wherein the digital matching logic includes a circuit to compare a reference scaled by a target code with a binary-weighted pull-up/pull-down structure.

6. The circuit of claim 5 wherein the digital matching logic includes a state machine to sample the comparison.

7. The circuit of claim 5 wherein the binary-weighted pull-up/pull-down structure has a fixed percentage minimum weighting.

8. The circuit of claim 1 wherein the digital matching logic includes a digital filter to reduce comparison related noise.

9. The circuit of claim 1 wherein the digital matching logic includes a rounding function to prevent hunting.

10. The circuit of claim 1 wherein each driver slice includes an uncompensated leg and a compensated leg.

11. The circuit of claim 2 wherein the uncompensated leg includes a circuit selected from a group comprising a pull-down circuit and a pull-up circuit.

12. The circuit of claim 2 wherein the compensated leg includes a circuit selected from a group comprising a pull-down circuit and a pull-up circuit.

13. The circuit of claim 2 wherein the compensated leg is compensated by an analog control voltage.

14. The circuit of claim 1 wherein the circuit is selected from a group comprising a driver and a buffer.

15. The circuit of claim 1 wherein the bias voltage matches pull-up to pull-down.

16. The circuit of claim 1 wherein the analog matching circuit operates independently from a number of driver slices.

17. The circuit of claim 1 wherein the bias voltage is distributed to all input/output (I/O) drivers.

18. The circuit of claim 1 wherein the pull-up and pull-down are compared at a given reference output voltage.

19. A method comprising:

providing a plurality of driver slices;

using a portion of the plurality of the driver slices to provide a target impedance;

providing digital matching logic to select the portion of the plurality of the driver slices; and

providing an analog matching circuit to produce a bias voltage to match pull-up and pull-down.

20. The method of claim 19 wherein the digital matching logic selects the portion of the plurality of the driver slices based on one or more items selected from a group comprising a target impedance and a reference resistor.

21. The method of claim 20 wherein the target impedance is determined through a dial-in code.

22. The method of claim 20 wherein the target impedance is selected based on one or more items selected from a group comprising a calibrated source and a look-up table.

23. The method of claim 19 wherein the digital matching logic compares a reference scaled by a target code with a binary-weighted pull-up/pull-down structure.

24. The method of claim 23 wherein the digital matching logic samples the comparison.

25. The method of claim 23 wherein the binary-weighted pull-up/pull-down structure has a fixed percentage minimum weighting.

26. The method of claim 19 wherein the digital matching logic provides a digital filter to reduce comparison related noise.

27. The method of claim 19 wherein the digital matching logic prevents hunting.

28. A computer system comprising:

a central processing unit (CPU);

a display device coupled to the CPU to display an image;

a plurality of driver slices, a portion of the plurality of the driver slices being used to provide a target impedance;

a digital matching logic to select the portion of the plurality of the driver slices; and

an analog matching circuit to produce a bias voltage to match pull-up and pull-down.

29. The computer system of claim 28 further including a main memory coupled to the CPU.

30. The computer system of claim 28 further including a memory coupled to the display device to store the image.